REMARKS

In response to the Office Action mailed March 28, 2003, Applicant respectfully requests reconsideration of this application, as amended, and consideration of the following remarks.

Amendments

Amendments to the Claims

Applicant has amended the claims to clarify that Applicant's invention uses a sole memory controller or means to manage memory for both a processing unit and a graphics subsystem. No new matter has been added as a result of these amendment.

Rejections

Rejections under 35 U.S.C. § 103

Claims 1-3, 5, 10-12, 15-16, 18, and 22-24

Claims 1-3, 5, 10-12, 15-16, 18, and 22-24 stand rejected under 35 U.S.C. § 103(a) as being obvious over Stortz (U.S. Patent 5,900,885) in view of Asaro et al. (U.S. Patent 6,100,906) and further in view of Chan et al. (U.S. Patent 6,184,908 B1), newly cited. Chan qualifies as prior art only under 35 U.S.C. § 102(e) based on its issue date of February 6, 2001 and Applicant reserves the right to swear behind the reference at a later date.

Stortz discloses a video controller that controls video memory on a graphics card and can use a portion of system memory that has been de-allocated from the system memory controller as an incremental video buffer. Stortz does not teach or suggest that the portion of system memory can be re-allocated to the system memory controller. Thus, Stortz teaches using two different components to control memory in the system, a system memory controller to control the system memory used by the CPU and a video controller to control the video memory and the incremental video buffer.

Asaro discloses a video processing module that manages two buffers in a dedicated video memory. Separate system memory is controlled by the CPU. Thus, like Stortz, Asaro teaches using two different components to control memory in the system,

the video controller to control the dedicated video memory and the CPU to control the system memory.

Chan discloses a graphics command processor having dedicated memory that is used as a partitioned buffer and a command buffer. An application program executing on the CPU of the system stores commands and raw vertex data into a system memory for processing by the graphics command processor. A fetcher component of the graphics command processor retrieves the commands and raw vertex data from the system memory and stores them into two different partitions in the partitioned buffer for processing. The resulting commands and vertex data are stored in the command buffer for output to a graphics engine and eventual display. Thus, Chan, teaches using two different components, the CPU and the fetcher, to control the portion of system memory that holds the input to the graphics command processor. Furthermore, Chan teaches that the partitioned and command buffers are controlled by the graphics command processor, not the CPU.

In contrast, Applicant claims a sole memory controller, or means, that manages main memory between a graphics subsystem and a processing unit. None of the references alone or in combination teach or suggest using a sole memory controller to manage memory as claimed by Applicant. Furthermore, using only a single memory controller is not obvious as a design preference as asserted by the Examiner in the pending Office Action. Applicant respectfully reminds the Examiner that a finding of "obvious design choice" is improper where the claimed structure and its function are different from, and provide advantages over, the prior art. *In re Chu*, 66 F.3d 202 (Fed. Cir. 1995). In particular, eliminating an element while retaining its function is indicative of non-obviousness [MPEP 2144.04(II)(B)]. Here, Applicant claims a single memory controller that performs the functions of two separate components in the prior art. Additionally, the advantages of a single memory controller over the separate components of the prior art are well-known to those of skill in unified memory architectures.

Furthermore, the Examiner admits that neither Stortz nor Asaro discloses Applicant's claimed element of partitioning an address space for a color buffer in main memory into two logical buffers and is relying on Chan's system memory as teaching this element. The Examiner stated that Chan's system memory is divided into two partitions

and the raw vertex data stored in the system memory contains color information. However, the only support for the statement Chan partitions system memory is that the commands and raw vertex data are shown as separate blocks in Figure 1. The section of Chan cited by the Examiner in support of his position describes storing the commands and raw vertex data into the different partitions in the partitioned buffer, not storing the command and raw vertex data into different partitions in the system memory. Even assuming Chan could be properly interpreted as partitioning system memory, Chan does not teach or suggest that the partition in system memory holding the raw vertex data is itself further partitioned into two additional logical partitions. Thus, Chan cannot be properly interpreted as disclosing Applicant's claimed element of partitioning an address space for a color buffer in main memory into two logical partitions

Moreover, the phrase "color buffer" is a term of art commonly defined as a pixel buffer that holds color attribute data, and optionally z-buffer data, and Applicant has used the term consistently with its common definition. Chan's raw vertex data is not equivalent to pixel color attribute data or z-buffer data. While claims must be interpreted broadly during prosecution, it is improper to interpret claim terms differently than their standard meaning unless the specification provides the different definition. Therefore, no partition holding raw vertex data in Chan's system can be properly interpreted as equivalent to Applicant's claimed address space for a color buffer.

Accordingly, the combination of Stortz, Asaro and Chan cannot render obvious Applicant's invention as claimed in claims 1-3, 5, 10-12, 15-16, 18, and 22-24, and Applicant respectfully requests the withdrawal of the rejection of the claims under 35 U.S.C. § 103(a) over the combination.

SUMMARY

In view of the foregoing amendments and remarks, Applicant respectfully submits that the pending claims are in condition for allowance. Applicant respectfully requests reconsideration of the application and allowance of the pending claims.

If the Examiner determines the prompt allowance of these claims could be facilitated by a telephone conference, the Examiner is invited to contact Sue Holloway at (408) 720-3476.

Deposit Account Authorization

Authorization is hereby given to charge our Deposit Account No. 02-2666 for any charges that may be due. Furthermore, if an extension is required, then Applicant hereby requests such an extension.

Respectfully submitted,

BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN

Date: 6/30, 2003

James C. Scheller, Jr.
Reg. No. 31,195

12400 Wilshire Boulevard
Seventh Floor
Los Angeles, California 90025-1026
(408) 720-8300

FIRST CLASS CERTIFICATE OF MAILING (37 C.F.R. § 1.8(a))

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail with sufficient postage in an envelope addressed to the Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450 on: June 30, 2003
Date of Deposit

Connie Thayer
Name of Person Mailing Correspondence

Connie Thayer
Signature

6-30-03
Date